CLAIMS

1. A serial binary multiplier for multiplying two binary operands to provide a final product, the multiplier comprising means for storing at least one first operand, a register for storing a partial product of the multiplication operation, means for receiving elements of a second operand serially, a calculation unit for calculating all possible results being the sum of the partial product and the product of the first operand with all possible values of the element of the second operand, said possible results being calculated during transmission of the second operand, means for selecting either one of the possible results or the currently stored partial product on the basis of the value of the received element of the second operand, means for shifting the partial product in the register to provide a new partial product, and means to output the contents of the register as the final product when all bits of the second operand have been received.

2. A serial binary multiplier according to claim 1, wherein the elements of the second operand are m-bit words.

3. A serial binary multiplier according to claim 2, wherein m=1 and the calculation unit is an adder.

4. A serial binary multiplier according to claim 1, 2 or 3, wherein the calculation unit calculates all possible results on the basis of the value of the first operand and the value of previously received elements of the second operand.

5. A serial binary multiplier according to any preceding claim, wherein the means to output the contents of the register provides the final result in serial form.

6. A serial binary multiplier according to any preceding claim, wherein the first and second operands and the final product are in two's complement form and the

possible results are calculated from the first operand, the partial product and the previously received bit of the second operand.

7. A serial binary multiplier according to claim 6, wherein the calculation unit is an adder and subtractor.

8. A serial binary multiplier according to claim 7, wherein the calculation unit is a single circuit capable of addition and subtraction, the operation being determined by the value of the previously received bit.

9. A method of operating a serial binary multiplier for multiplying two binary operands to provide a product comprising the steps of storing a first operand, storing a partial product in a register, transmitting elements of a second operand serially whilst simultaneously calculating all possible results being the sum of the partial product and the product of the first operand with all possible values of the element of the second operand, selecting either one of the possible results or the currently stored partial product on the basis of the value of the received element of the second operand, shifting the partial product in the register to provide a new partial product, and outputting the contents of the register as the final product when all bits of the second operand have been received.

10. A serial binary multiplier substantially as hereinbefore described with reference to the accompanying drawings.

11. A method of operating a serial binary multiplier substantially as hereinbefore described with reference to the accompanying drawings.

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